JOLT

First Edition

Microcomputer Associates Inc.
Santa Clara, California

Introduction

The Jolt is one of the first 6502 based SBCs produced by Micro Associates in 1975.

This User Manual is derived from the Super Jolt Manual, 1977 by Micro Associates.

The relevant parts for the Jolt are kept. Enhanced with the circuit diagram and PCB layouts of the Jolt Replica by Eduardo Casino.

Refer to the Demon/TIM manual for more information on the 6530-004 TOM IC that has the operating system monitor and hardware description.

Hans Otten, 2026

SECTION 1

START-UP

HOOKING UP THE POWER SUPPLY

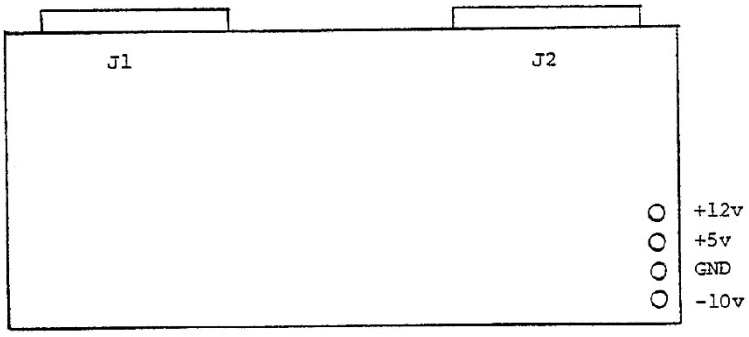
The proper power supply is an important part of your JOLT system. Be sure to check your power source and have identified the proper connections and have tested the power supply to be certain that all voltages are proper and that none have overvoltage surges when TURNING ON power.

Your JOLT card requires a minimum of two voltages and one ground connection. The card, as delivered will perform with +5v, GND, and -10v if you are using the TTY current loop. If you plan to use the EIA terminal connection you will need to add the +12v supply. Power supply requirements are listed below.

POWER SUPPLY REQUIREMENTS

	TYPICAL		MAXIMUM	
Voltage				
+12v±5%		4.4 ma		6 ma
+5v±5%		520 ma		850 ma
-10v±5%		30 ma		40 ma

All power connections are hooked up as indicated below and as marked on the P.C. card.



HOOKING UP A TERMINAL TO THE JOLT

Types of Terminals: The following is a list of qualifications a terminal must have to run on a JOLT system with DEMON™ installed:

A. Character Set: Must transmit and receive the standard ASCII character set. (64, 96, or 128 character).

B. Mode: Mode of transmission is bit serial full duplex (full duplex is where the keyboard sends only to the computer and the computer sends only to the printer).

C. Transmission Rate: Transmission rate can be anything from 110 to 300 baud (10 to 30 characters per second) the SUPER JOLT will synchronize to the baud rate of the terminal.

D. Bit Serial Format: Start bit, seven data bits, one parity bit (this bit is ignored by DEMON™ on receive and set to a "1" on transmit), and one, one and a half, or two stop bits.

E. Electrical Interface: Any one of three types of electrical interfaces can be used with the SUPER JOLT

1. RS-232C (EIA)
2. 20 milliamp current loop interface
3. TTL logic interface

HOOKING UP THAT ELECTRICAL INTERFACE

E.I.A.: The first type of interface we will discuss is the E.I.A. or RS-232C standard, here after refered to as E.I.A.. Table 1 shows the complete standard for signal assignment on the 25 Pin Cannon connector which is the standard connector for terminal-modem computer hookup with E.I.A.. Figure 1 shows the connection of a typical E.I.A. terminal to the JOLT CPU. When using the with an E.I.A. interface equipped terminal, connections should be made in this fashion. Note that the D.S.R. signal from the CPU is required only on some terminals.

TTY CURRENT LOOP

The most common example of a current loop interfaced terminal is the model ASR33 Teletype™. Before hooking up your Teletype™ or other current loop type terminal

RS-232 STANDARD SIGNALS AT THE TERMINAL

* Signals Commonly Used

PIN	FUNCTION
*1	Protective ground
*2	Transmitted data
*3	Received data
4	Request to send
5	Clear to send
6	Data set ready
*7	Signal ground
8	Data carrier detector
9	Reserved for data set testing
10	Reserved for data set testing
11	Unassigned
12	Unassigned
13	Unassigned
14	Unassigned
15	Unassigned
16	Unassigned
17	Unassigned
18	Unassigned
19	Unassigned
20	Data terminal ready
21	Unassigned
22	Ring indicator
23	Unassigned
24	Unassigned
25	Unassigned

TABLE 1

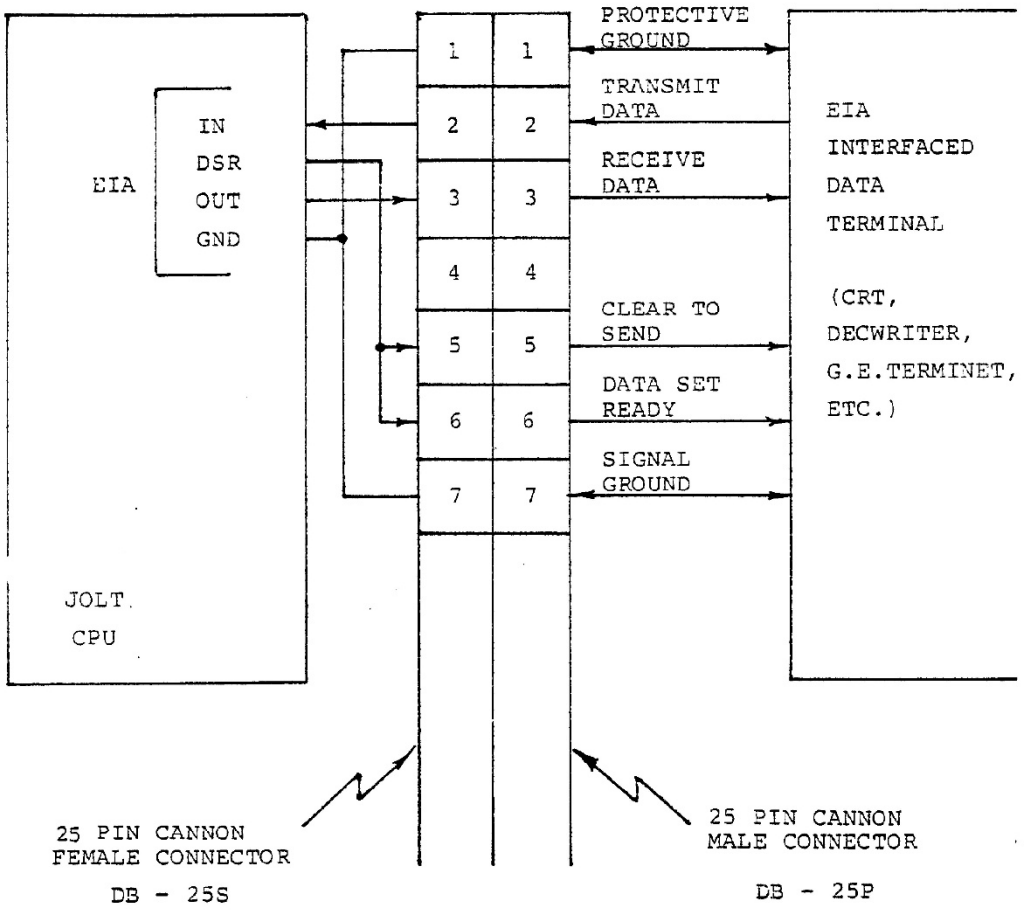
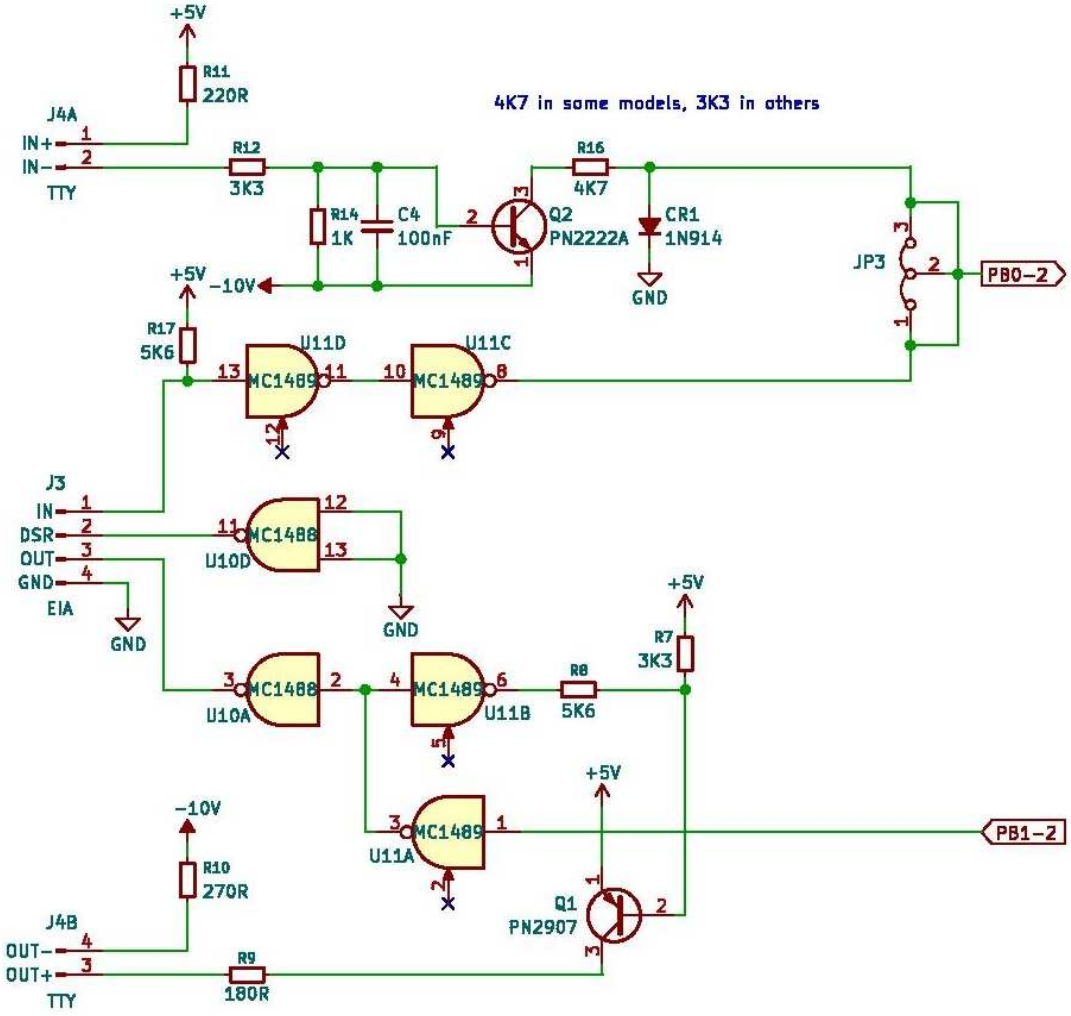


FIGURE 1. JOLT HOOKED TO AN EIA EQUIPPED TERMINAL

refer to its maintanence manual and be certain that it is set up for 20 milliamp current loop operation and identify the four interface wires shown in Figure 2 for the Teletype™. If your Teletype™ also has a paper tape reader, then check to see that it is an automatic reader as JOLT does not supply a "reader run" relay control circuit.

Unlike RS-232C, the 20 milliamp current loop interface has no standard connector. Every computer and terminal manufacturer has their own type of connector. For interfacing the JOLT you should select a connector that mates with the one on your particular model Teletype™.

Figure 2 shows a typical teletype hookup to JOLT using the 20 milliamp current loop interface.



The part of the Circuit that shows the serial interfaces.

Note the jumper JP3 to select EIA or 20mA current loop.

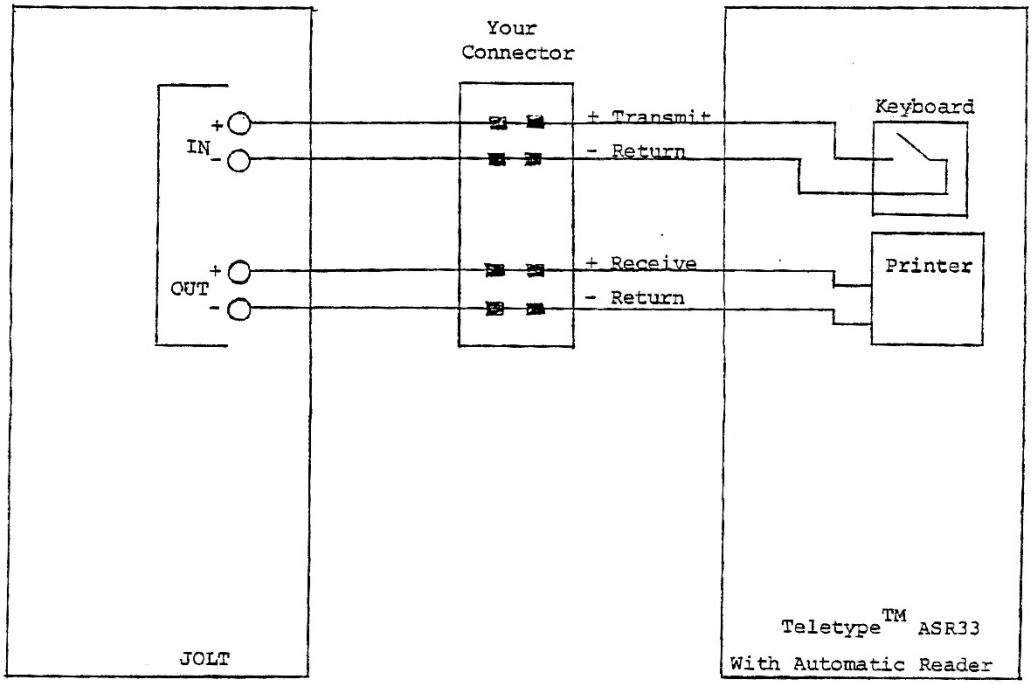


FIGURE 2. JOLT HOOKED TO A 20 ma CURRENT LOOP TELETYPE™

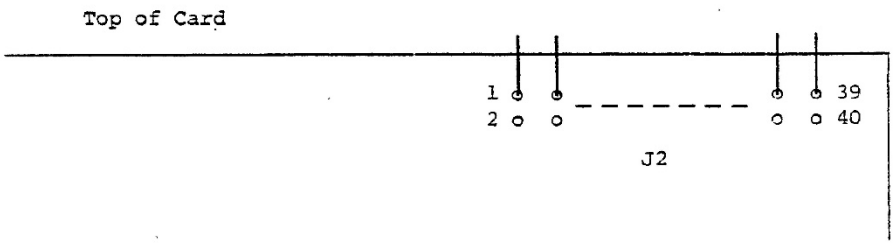
READY TO RUN?

Your SUPER JOLT card comes ready to power-up automatically to the on-board debugger-monitor DEMON™ using a TTY. Refer to section 4 on using DEMON™

Again, if you have a TTY (20 ma current loop) and a power supply your JOLT is ready-to-use with no jumper changes. Power-up or reset will cause the 6502 CPU to execute the DEbug MONitor.

HOOKING UP THE I/O

JOLT is designed with two types of connectors. The first, called J1, is on the upper left and is used mainly for system expansion such as RAM, PROM, I/O etc. J1 should only be used to expand to other available JOLT cards or for your own special card designs. The second, called J2, is on the upper right and contains all on-board I/O lines. Table 2 list J2 I/O pin #'s and software address assignments and Table 3 list available mating connectors. Pin numbering on both connectors is illustrated as follows:



PART #1	Bit #	NAME	PIN #	ADDRESS
	0	PA0-1	31	
	1	PA1-1	32	6520 PIA
	2	PA2-1	30	4600 Direction/Data
	3	PA3-1	29	4601 Control
	4	PA4-1	28	
	5	PA5-1	27	
	6	PA6-1	33	
	7	PA7-1	34	
	Interrupt Input	CA1-1	38	
	Output Control	CA2-1	39	

PORT #2	BIT #	NAME	PIN #	
	0	PB0-1	35	
	1	PB1-1	36	6520 PIA
	2	PB2-1	37	4602 Direction/Data
	3	PB3-1	26	4603 Control
	4	PB4-1	25	
	5	PB5-1	24	
	6	PB6-1	23	
	7	PB7-1	22	
	Interrupt Input	CB1-1	21	
	Output Control	CB2-1	20	

PORT #3	BIT #	NAME	PIN #	
	0	PA0-2	10	
	1	PA1-2	15	6530 I/O
	2	PA2-2	16	6E00 Data
	3	PA3-2	17	6E01 Direction
	4	PA4-2	18	
	5	PA5-2	19	
	6	PA6-2	14	
	7	PA7-2	13	

PORT #4	BIT #	NAME	PIN #	
	2	PB2-2	12	6E02 Data
	3	PB3-2	11	6E03 Direction

TABLE 2. SUPER JOLT I/O ASSIGNMENTS ON J2

FOR FLAT CABLE CONNECTIONS

T & B ANSLEY P/N: 609-4000

SPECTRA-STRIP P/N: 802-140

3M P/N: 3417-0000

FOR P.C. MOUNTING

AMP P/N: 86418-2

FLAT CABLING

T & B ANSLEY P/N: 171-40

SPECTRA-STRIP: Many Types

3M P/N: 3302/40, 3365/40, 3469/40, 3476/40

TABLE 3. J1 & J2 MATING CONNECTOR

SECTION 2

JOLT MODULE

General

The JOLT CPU card is a complete microcomputer on a single printed circuit board. When connected to a terminal, the CPU card provides everything necessary to begin writing, debugging and executing microcomputer programs. The salient features of the SUPER JOLT CPU card are:

- A MOS Technology MCS6502 NMOS microprocessor
- 1024 bytes of program RAM, and 64 bytes of interrupt vector RAM
- 1024 bytes of mask programmed ROM containing DEMON™, a powerful debug monitor
- 28 programmable I/O lines
- Crystal controlled clock
- Serial I/O ports for use with a teleprinter current loop drive/receiver, EIA standard driver/receiver, or TTL
- Expandable address and data buses
- Buffered CPU address and data lines
- Hardware interrupts
- Control panel interface lines available on card connector

The CPU card was designed to be a general purpose microcomputer with provisions for expanding memory and interfacing to serial or parallel I/O devices. System expansion may be accomplished through the use of standard JOLT support cards.

CPU

The MCS6502 CPU chip is a parallel 8-bit NMOS microprocessor with 16 address lines and an internal oscillator. The data bus (D0-D7) is bi-directional and will drive one TTL (1.6 ma, 130 pf) load directly. The 64K byte (2^{16}) address space is used to address program memory and to select I/O devices for communication with the CPU. The address will also drive one TTL (1.6 ma, 130 pf) load directly. On-board address and data buffers expand the drive capability to 48 ma.

The internal oscillator operates in a "free run" mode based on a crystal oscillator frequency of 1 MHZ. The crystal provides a very stable clock which allows for accurate and repeatable programmed timing loops.

The RESET input to the CPU is pulled to logic ground by a 555 timer circuit on the printed circuit board. The CPU normally fetches a new program count vector from hex locations FFFC and FFFD upon activation of the RESET line, but these locations are in the interrupt vector RAM and therefore volatile. Hardware on the CPU board causes the CPU to begin executing the monitor program by forcing the effective sixteenth bit of the address bus (A15) to a logic ZERO during reset. As a result, the RESET function on the SUPER JOLT CPU card cause the debug monitor (DEMON™) to begin executing. This can be altered by changing the various on-board jumpers. (see section 3)

There are two interrupt inputs to the CPU. One interrupt is maskable under program control ($\overline{IRQ}$) and the other ($\overline{NMI}$) is not.

A READY control line provides for asynchronous operation with slow memory or I/O devices.

The address bus (A0-A15), the data bus (D0-D7), the two phase clock (P1T,P2T), the reset line (*RESET), the interrupt lines (*IRZ, and *NMI) and the ready line (RDY) are all available at the edge connector of the CPU card.

A more detailed description of the CPU inputs and outputs may be found in the MCS6500 hardware manual available from MOS Technology Inc.

PROGRAM RAM

There are 1024 bytes of program RAM provided on the CPU card. The program RAM is hardwired addressed as the first 1024 bytes of the CPU's 64K of memory address space. It may become necessory to remove these RAM's from their sockets if a 4K memory card is also hardwired in this address space. The program RAM on the CPU card uses 2114 4K static RAMs.

MONITOR ROM AND INTERRUPT VECTOR RAM

The monitor ROM is located in the last 1K bytes of the lower half of memory space (first 32K bytes). The interrupt vector RAM is located in the last 64 bytes of the 64K memory address space.

The monitor ROM and interrupt vector RAM as well as additional I/O are implemented with a single MPS6530 chip.

PROGRAMMABLE USER I/O

The programmable I/O lines available from the CPU card are provided by a Peripheral Interface Adapter (PIA) and the 6530 multi-function chip.

The PIA has two 8-bit I/O ports with two interrupt-causing control lines each. A data direction register for each port determines whether each I/O line is an input or an output. A detailed description of the PIA chip may be found in the MCS6500 microcomputer family Hardware Manual.

The 6530 ROM chip provides 10 additional I/O lines that may also be specified as input or output lines under program control. There are eight I/O lines from one port on the 6530 and two lines from the second port. These I/O lines may be used in conjunction with DEMON™ for interfacing a high speed paper tape reader to the CPU card. In the paper tape reader application, the eight I/O lines from the second port are used to accomplish the handshake control between the reader and the CPU card.

The PIA is hardwired addressed as location $5C00_{16}$ to $5C03_{16}$ in the memory address space. Memory addresses from 4000_{16} to $5C03_{16}$ are allocated for PIA devices so that the JOLT system may be easily expanded to accomodate up to eight PIA chips. For a complete illustration of memory allocation refer to section 3.

STANDARD INTERFACE CIRCUITS

The JOLT CPU card provides direct interfacing with a 20 ma current loop RS232C interface requires +12v and -10v. Both interfaces are wired in parallel on the input and output thereby allowing both interfaces to be used simultaniously.

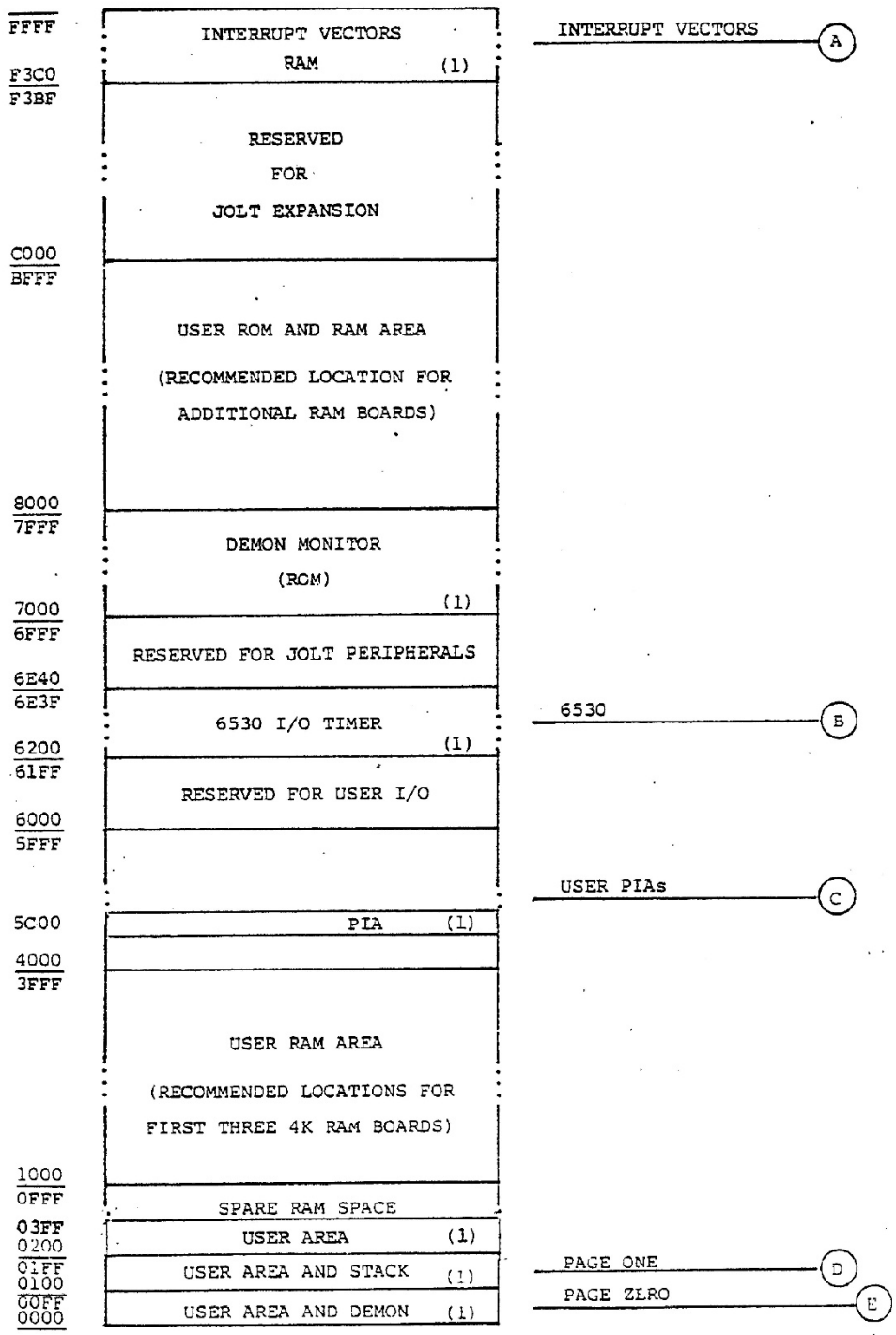
SECTION 3

MEMORY MAP

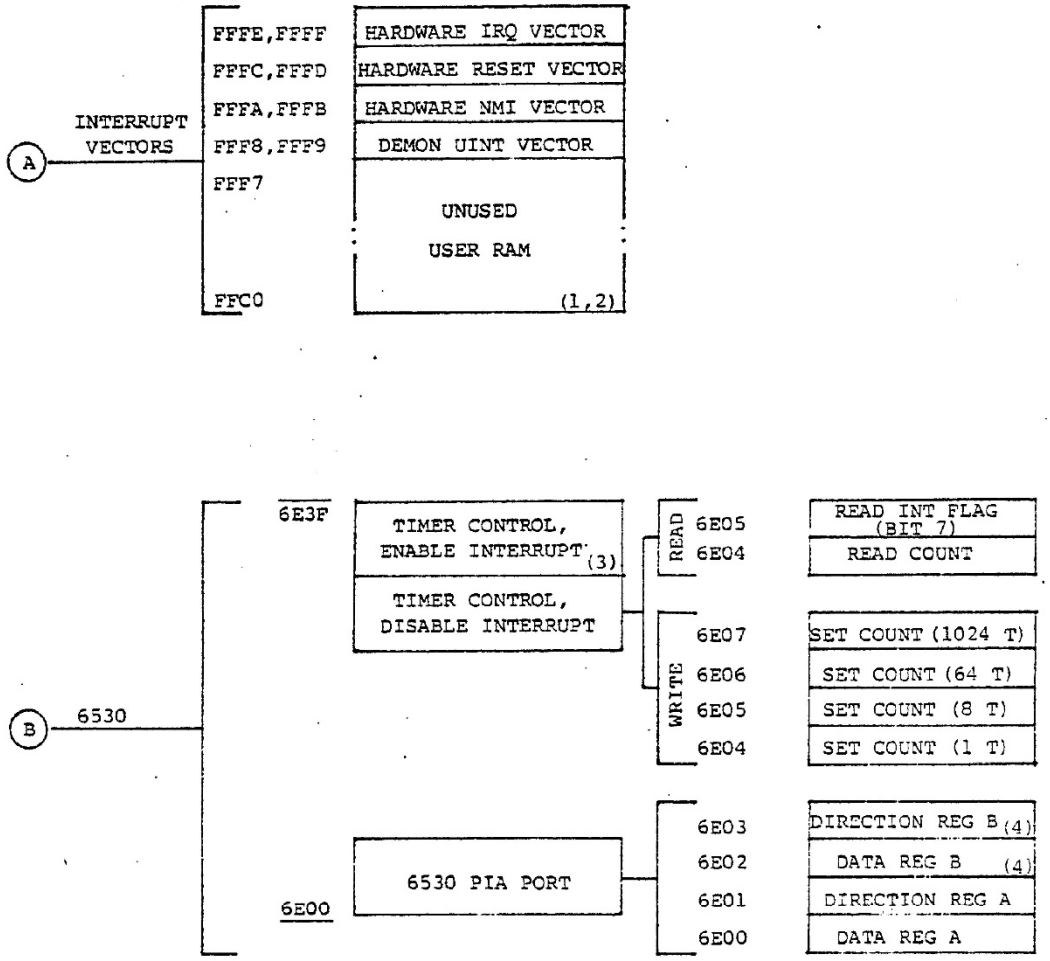
JOLT SYSTEM MEMORY MAP

The memory map on the following pages explains what functions have been assigned to each segment of the SUPER JOLT address space. It is recommended that users respect this space allocation when adding memory and peripherals to their JOLT systems. Space has been reserved for 32K bytes of user RAM or ROM, seven additional PIA devices, and up to 512 user I/O devices registers. Other areas are reserved for JOLT expansion, i.e., new SUPER JOLT peripherals and memory options will use these spaces. Users are advised to not use SUPER JOLT expansion space unless absolutely necessary.

Note that some areas used by the JOLT CPU board and PIA boards have more space indicated than there are registers or locations in the device occupying them. This is because these devices do not decode all address bits, or use some of the address bits for special functions. For example, the 6530 timer determines the time scale and interrupt enable/disable by the address used to access it. Thus, these "partly filled" areas are actually entirely used and are not available for other uses.



(1) Standard on JOLT CPU Card

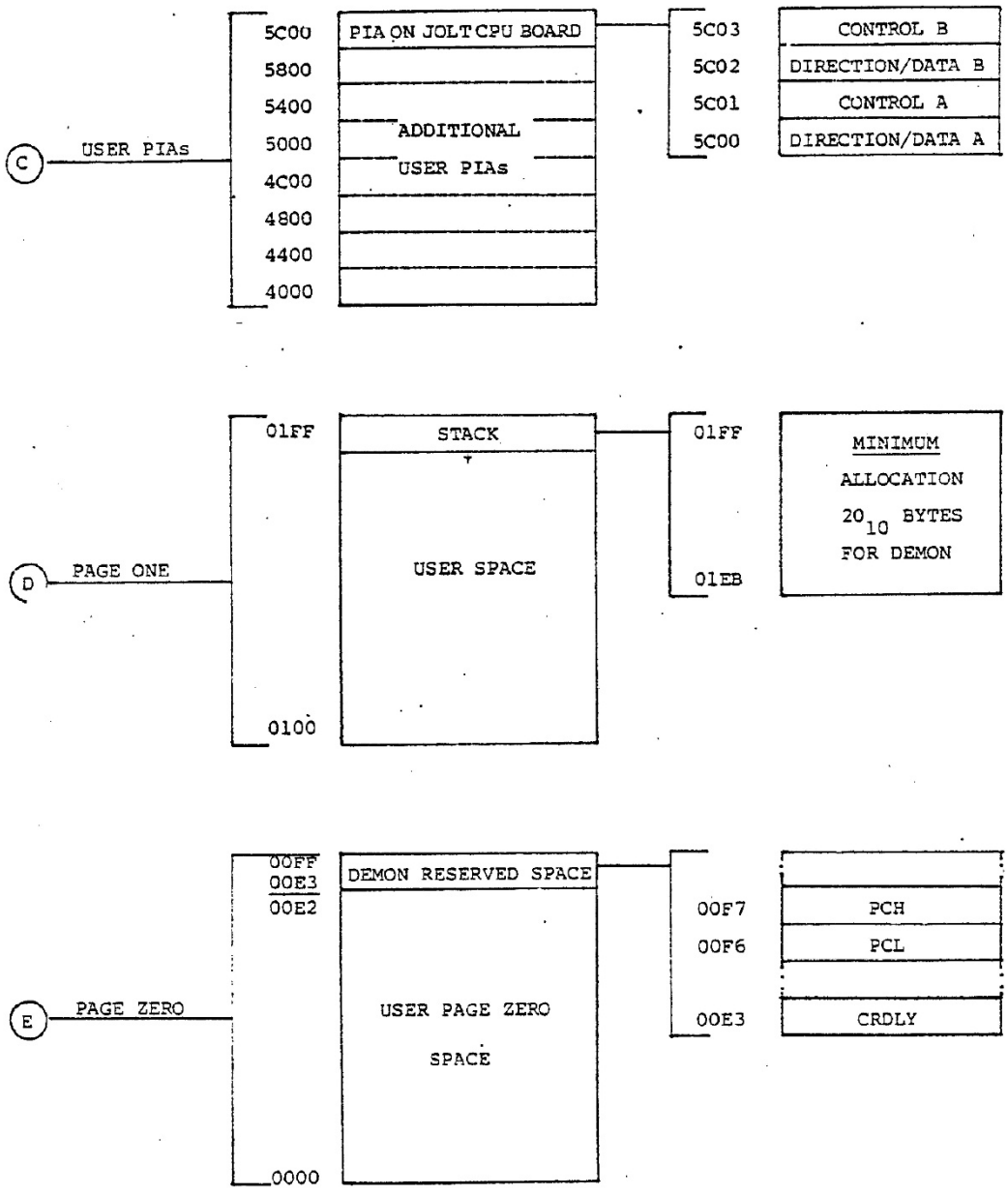


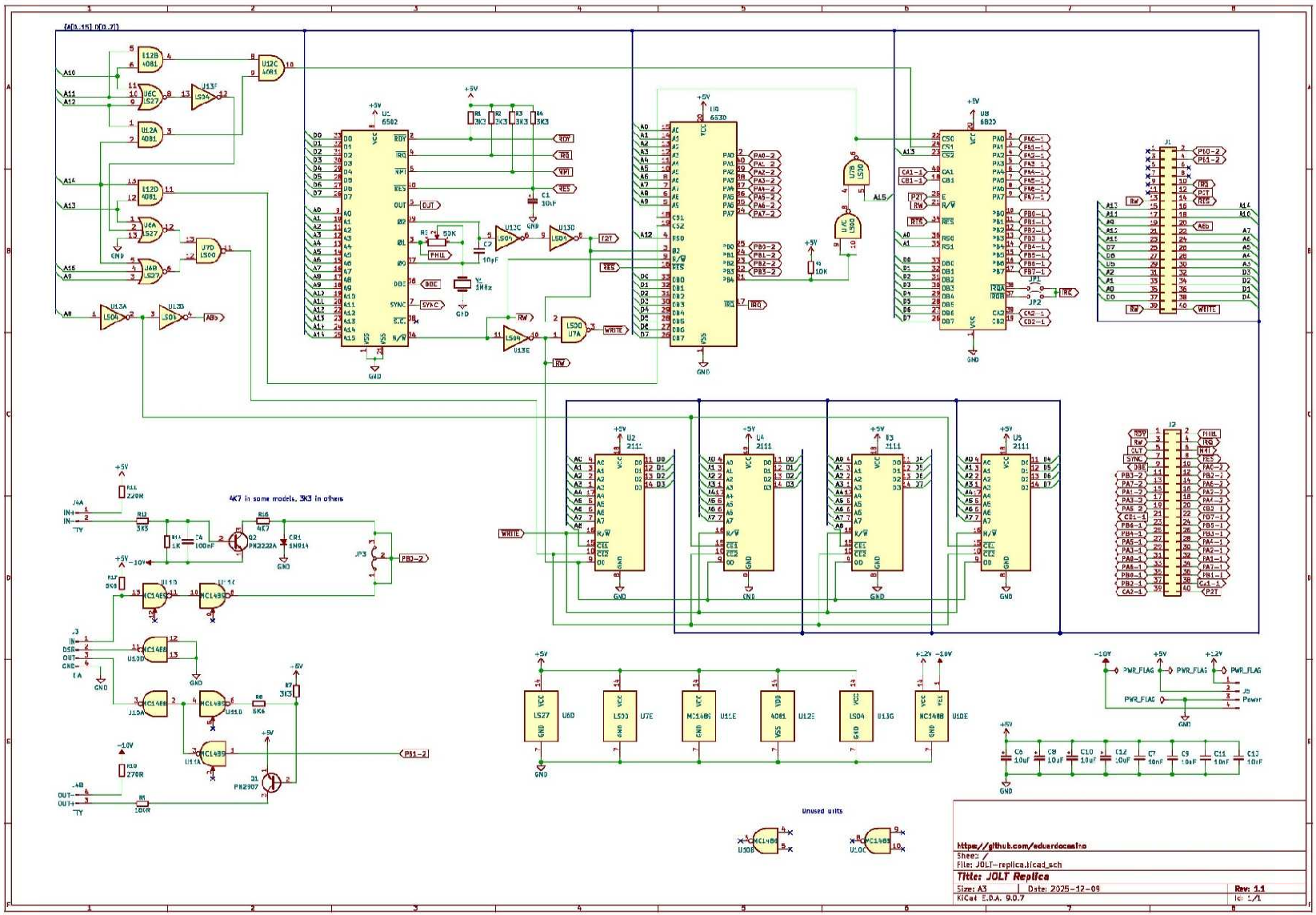
(1) Standard on JOLT CPU board.

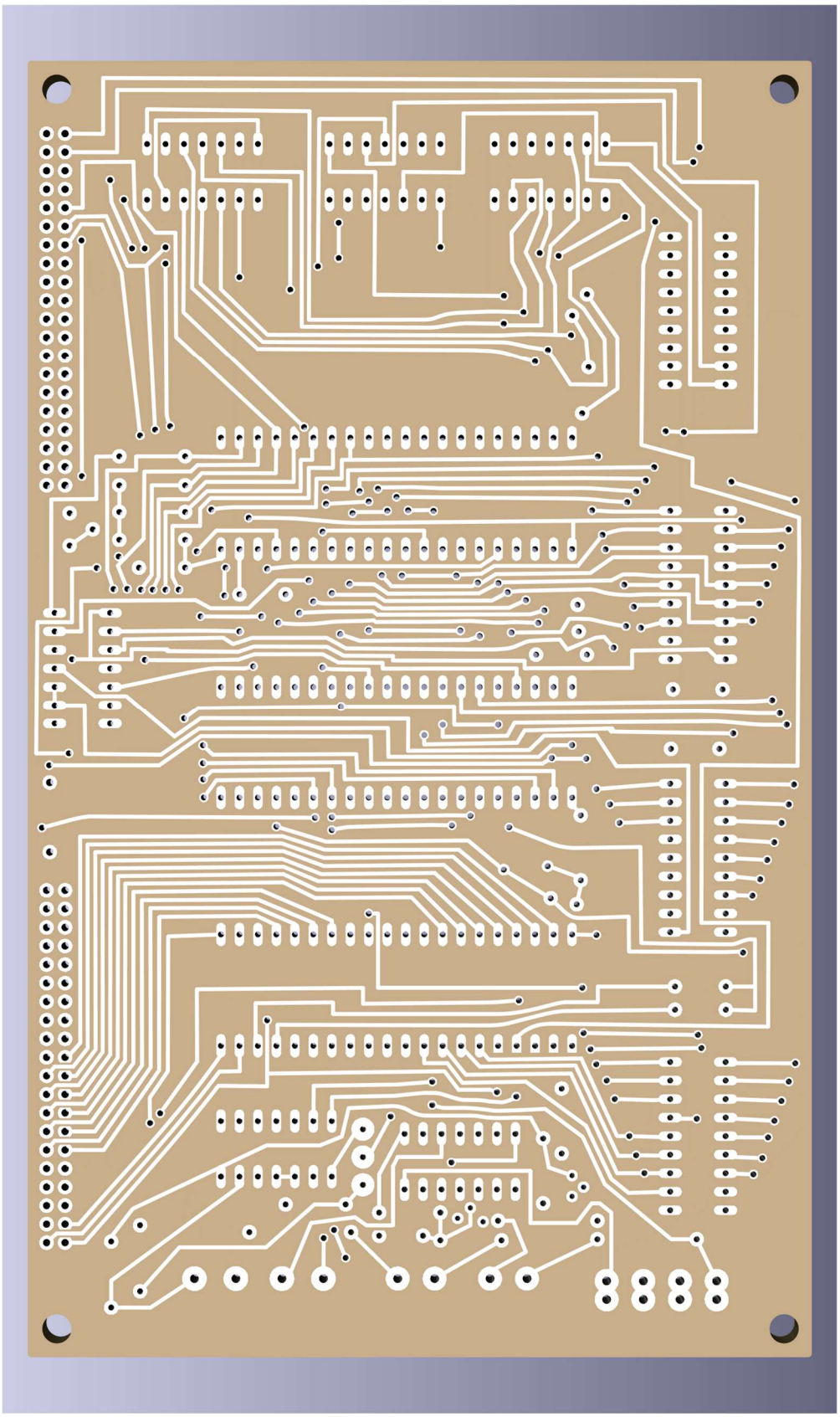
(2) Available to user—not used by DEMON.

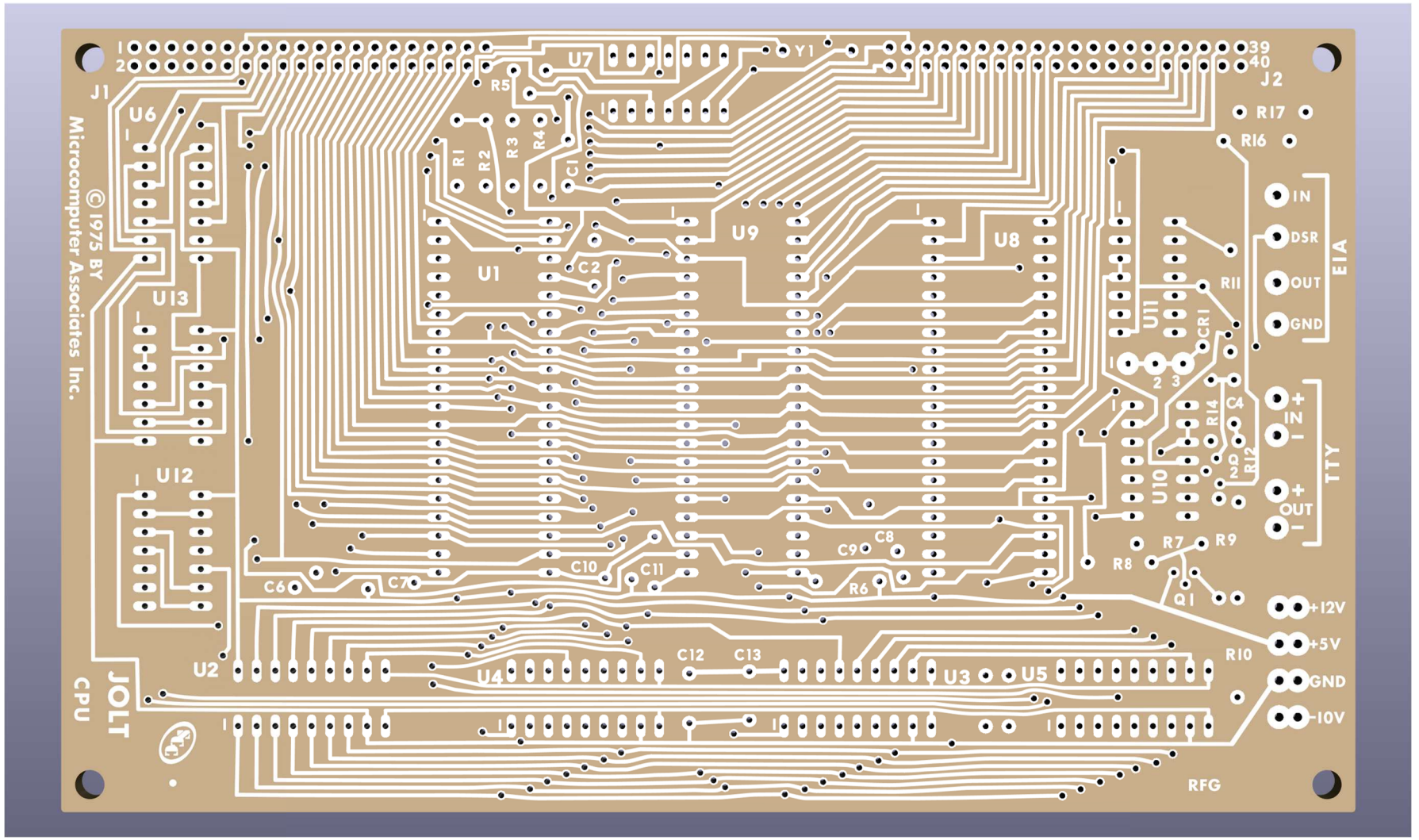
(3) To get enable-interrupt address, add 0008_{16} to disable-interrupt address with corresponding functions.

(4) Reserved for DEMON use—TTY control and reset functions.


C
USER PIAs
5C00
5800
5400
5000
4C00
4800
4400
4000
PIA ON JOLT CPU BOARD
ADDITIONAL
USER PIAs
5C03
5C02
5C01
5C00
CONTROL B
DIRECTION/DATA B
CONTROL A
DIRECTION/DATA A
D
PAGE ONE
01FF
0100
STACK
USER SPACE
01FF
01EB
MINIMUM
ALLOCATION
20_{10} BYTES
FOR DEMON
E
PAGE ZERO
00FF
00E3
00E2
0000
DEMON RESERVED SPACE
USER PAGE ZERO
SPACE
00F7
00F6
00E3
PCH
PCL
CRDLY


4K7 in some models. 3K3 in others
Unused units
https://github.com/eduardocasino
Sheet: /
File: JOLT-replica.kicad_sch
Title: JOLT Replica
Size: A3
Date: 2025-12-09
Rev: 1.1
KiCad E.D.A. 9.0.7




J1
J2
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
Y1
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R14
R16
R17
C1
C2
C4
C6
C7
C8
C9
C10
C11
C12
C13
CR1
Q1
IN
DSR
OUT
GND
EIA
IN
OUT
TTY
+12V
+5V
GND
-10V
JOLT
CPU
RFG
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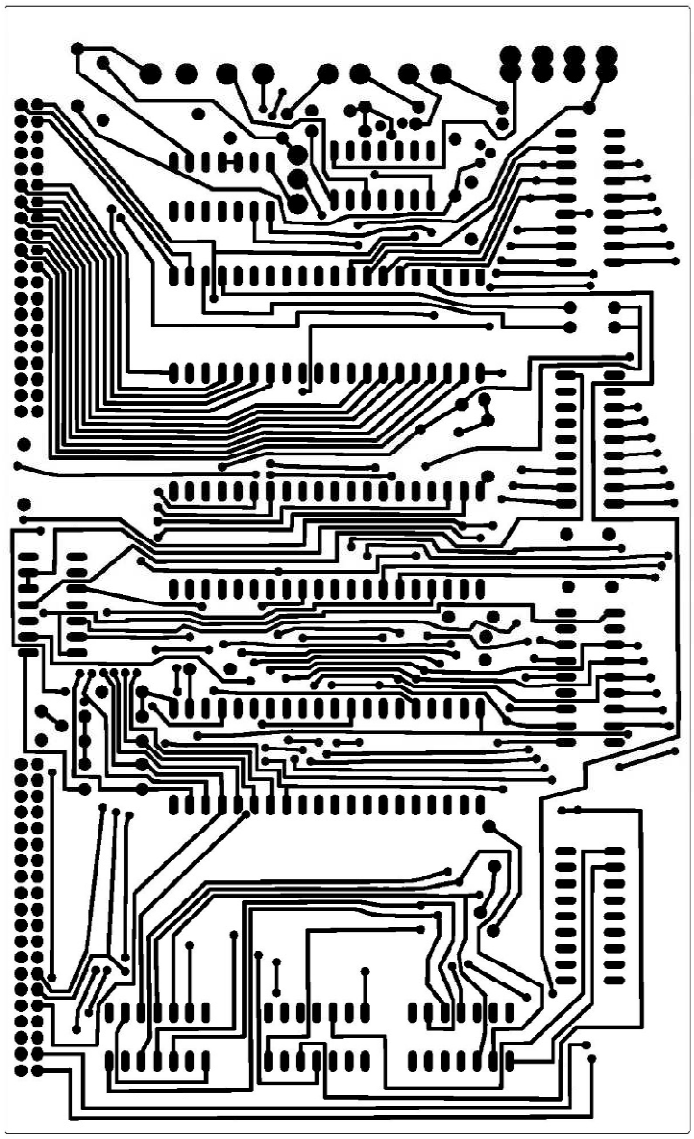

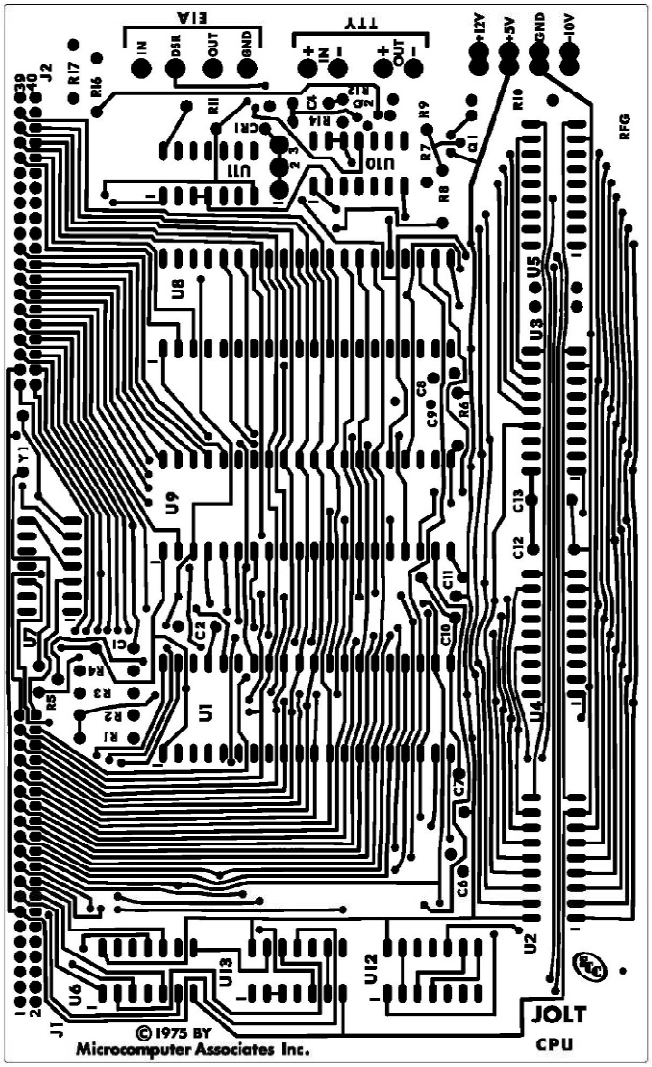
EIA
IN
DSR
OUT
GND
TTY
IN
OUT
+12V
+5V
GND
-10V
J2
J1
U1
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U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
Y1
C1
C2
C6
C7
C8
C9
C10
C11
C12
C13
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
Q1
CR1
RFG
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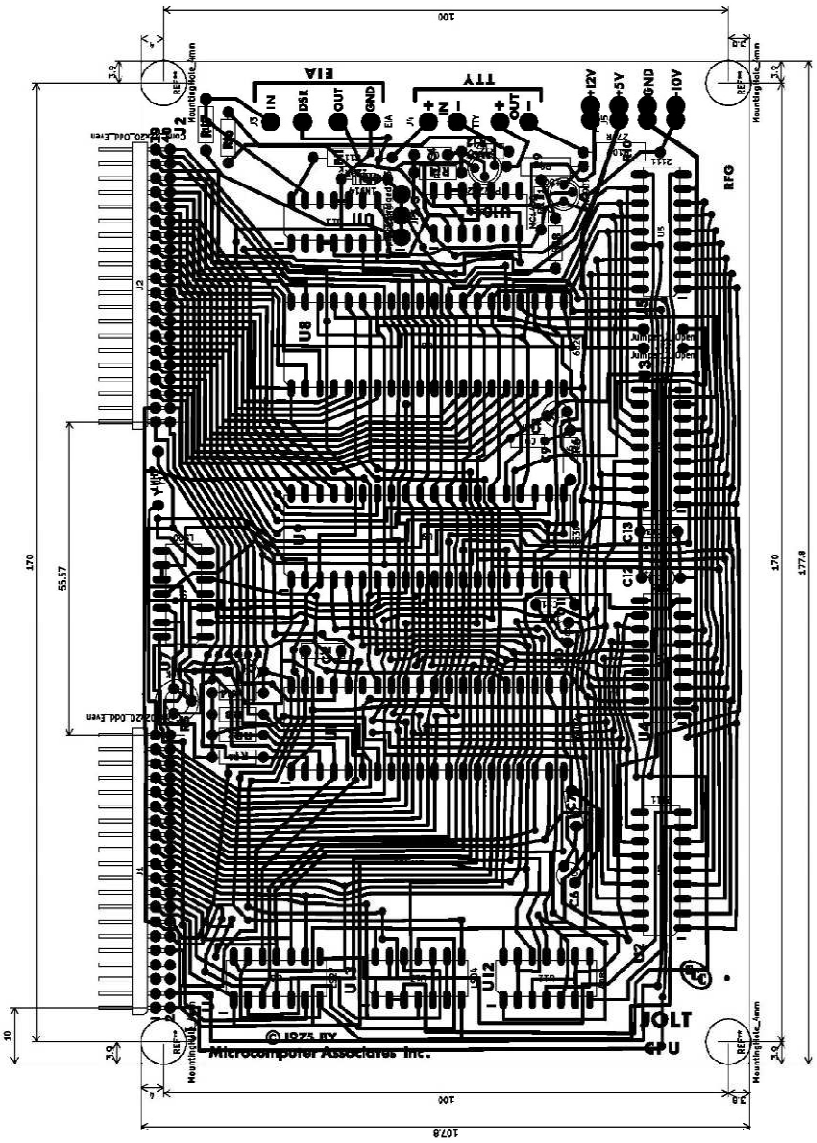
JOLT
CPU


EIA
TTY
+12V
+5V
GND
+10V
IN
DSR
OUT
GND
Microcomputer Associates Inc.
VOLT
CPU
100
170
55.17
177.8
107.8